Title:

NEW TDMA6-641 DOWNLINK baseline definition.

Source:

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Abstract:

In this contribution we describe a modified baseline scheme for the Downlink TDMA Half Rate mode with IS-641 Acelp (i.e. TDMA6-641). The resulting system is similar to the one presented in [1], but assigns two separate CRC to the two users that are sharing the same downlink slot. We give error performance curves, and we show that this modified scheme achieves similar performance to the scheme in [1].

Recommendation:

Review and adopt as TDMA6-641 downlink baseline

Notices:

Introduction

In [2] it is specified that Half Rate shall demonstrate that Voice Privacy will be maintained per user. We addressed this problem in [3], where we showed that this requirement can be fulfilled if the information streams of users that share the same slot are separately CRC protected and channel encoded. In [1] we already presented a proposal for the definition of the Downlink TDMA Half rate mode with IS-641 Acelp vocoder. However, the scheme in [1] does not fulfill the aforementioned requirement. Here we show that it is possible to slightly modify the scheme in [1] and fulfill [2], using the approach described in [3]. We refer to the Half Rate mode using IS-641 Acelp codec and the modification here described as TDMA6-641-NEW. As in [1] pair of users are allocated in one slot (two users channel co-sharing), and are then interleaved across two slots separated by 20 ms (fig.1). Now, differently from [1], co-shared users are protected with separate CRC bits, and are then independently convolutional encoded. In the following sections we give the implementation details of TDMA6-641-NEW in terms of: bit partitions, channel coding, scrambling, interleaving, and finally mapping.

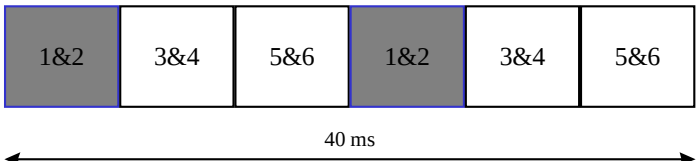

Fig. 1: Frame format and slot allocation to users in TDMA6-NEW Downlink with slot co-sharing among pair of users.

Bits partition at the Acelp vocoder output

A 20 ms speech buffer from each user is speech encoded as per IS-641. For the purpose of this contribution, random speech bits were used for each user. Thus, each user has 148 random output speech bits per 20 ms. These bits are partitioned in 48 class 1A, 48 class 1B, and 52 class 2 bits. The total amount of bits from 2 users in 20 ms is 296 : 96 class 1A, 96 class 1B, and 104 class 2.

Channel encoding

First, we separately add to class 1A bits of user 1 and to class 1A bits of user 2, 7 CRC bits for frame error detection purposes. Then we separately encode the 48+7 class 1A bits of user 1 and of user 2 with a tail biting convolutional code with constraint length K=6, rate 2/3. Thus we obtain 83 class 1A coded bits for user 1 (*a1(i)*, i=0,...,82) and other 83 bits for user 2 (*a2(i)*, i=0,...,82). Similarly, class 1B bits are separately protected each with a tail biting convolutional code with constraint length K=6, and rate 3/4. This produces 64 coded class 1B bits for user 1 (*b1(i)*, i=0,...,63) and 64 other bits for user 2 (*b2(i)*, i=0,...,63). These codes are obtained from a punctured rate ½ mother code. Code polynomials are shown in figure 2, while puncturing matrixes are shown in figure 3. Class 2 bits (*c1(i)*, i=0,...,51 of user 1 ; *c2(i)*, i=0,...,51 of user 2) are left uncoded. Finally the total number of bits at the output of the convolutional encoder (i.e. coded class 1A + coded CRC+ coded class 1B + class 2) is 398.

$$G_{k=6}=[\ 075 \quad 053\ ]$$

Fig. 2. Polynomials in octal representation.

$$\text{Class 1A: } \begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix}$$

$$\text{Class 1B: } \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 0 \end{bmatrix}$$

Fig. 3. Puncturing matrices for class 1A and class 1B bits.

Scrambling

Before reordering and interleaving, the coded bits of the 2 users are scrambled. In particular, coded class 1A bits of user 1 are scrambled with coded class 1A bits of user 2; coded class 1B bits of user 1 are scrambled with coded class 1B bits of user 2; class 2 bits of user 1 are scrambled with class 2 bits of user 2. Thus, indicating with *a1* the 83 class 1A bits of user 1, with *a2* the 83 bits of user 2, then the 166 scrambled bits of coded class 1A are *bC1A*:

$$bC1A(2i) = a1(i), \quad i = 0,1,...,82 \qquad bC1A(2i+1) = a2(i), \quad i = 0,1,...,82$$

Similarly, indicating with *b1* the 64 class 1B bits of user 1, with *b2* the 64 bits of user 2, then the 128 scrambled bits of coded class 1B are *bC1B*:

$$bC1B(2i) = b1(i), \quad i = 0,1,\ldots,63 \qquad bC1B(2i+1) = b2(i), \quad i = 0,1,\ldots,63$$

Finally indicating with *c1* the 52 class 2 bits of user 1, with *c2* the 52 bits of user 2, the 104 scrambled bits of class 2 are *bC2* :

$$bC2(2i) = c1(i), \quad i = 0,1,\ldots,51 \qquad bC2(2i+1) = c2(i), \quad i = 0,1,\ldots,51$$

It should be noted that coding and scrambling take place in reverse order to that in [1]. Furthermore, due to independent coding we obtain 398 bits. Since the downlink slot format has a payload of 399 bits, we choose to leave the 399th bit unused.

Reordering and Interleaving

After encoding and scrambling, the bits are arranged in priority order format (scrambled class 1 followed by scrambled class 2). The resulting vector of 399 bits is indexed from 0 to 398 and reordered using the matrix given in figure 4. Bits from 0 to 165 are coded class 1A + CRC, bits from 166 to 293 are coded class 1B, and finally bits from 294 to 397 are class 2. Bit 398 is set to zero. Inter-slot interleaving can now be accomplished simply transmitting in each time slot half of the bits that belong to the current speech frame and half the bits that belong to the previous speech frame. After reordering the bits, the odd-indexed rows (1,3,…,13) are exchanged with the corresponding rows from the next speech frame. Thus, the even indexed rows (0,2,…,12) are kept within the same slot, e.g. slot 1, but the odd-indexed (1,3,...,13) rows are placed in slot 4 of the next 20 ms frame.

Row 0	0,166,294,13,179,307,26,192,320,39,205,333,52,218,346,65,231,359,78,244,372,91,257,385,104,117,270, 130,136,142,148,153,158,163,285,290
Row 1	1,167,295,14,180,308,27,193,321,40,206,334,53,219,347,66,232,360,79,245,373,92,258,386,105,118,271, 131,137,143,149,154,159,164,286,291
Row 2	2,168,296,15,181,309,28,194,322,41,207,335,54,220,348,67,233,361,80,246,374,93,259,387,106,119,272, 132,138,144,150,155,160,165,287,292
Row 3	3,169,297,16,182,310,29,195,323,42,208,336,55,221,349,68,234,362,81,247,375,94,260,388,107,120,273, 133,139,145,151,156,161,283,288,293
Row 4	4,170,298,17,183,311,30,196,324,43,209,337,56,222,350,69,235,363,82,248,376,95,261,389,108,121,274, 134,140,146,152,157,162,284,289,398
Row 5	5,171,299,18,184,312,31,197,325,44,210,338,57,223,351,70,236,364,83,249,377,96,262,390,109,122,275, 135,141,147
Row 6	6,172,300,19,185,313,32,198,326,45,211,339,58,224,352,71,237,365,84,250,378,97,263,391,110,123,276
Row 7	7,173,301,20,186,314,33,199,327,46,212,340,59,225,353,72,238,366,85,251,379,98,264,392,111,124,277
Row 8	8,174,302,21,187,315,34,200,328,47,213,341,60,226,354,73,239,367,86,252,380,99,265,393,112,125,278
Row 9	9,175,303,22,188,316,35,201,329,48,214,342,61,227,355,74,240,368,87,253,381,100,266,394,113,126,279
Row 10	10,176,304,23,189,317,36,202,330,49,215,343,62,228,356,75,241,369,88,254,382,101,267,395,114,127,280
Row 11	11,177,305,24,190,318,37,203,331,50,216,344,63,229,357,76,242,370,89,255,383,102,268,396,115,128,281
Row 12	12,178,306,25,191,319,38,204,332,51,217,345
Row 13	64,230,358,77,243,371,90,256,384,103,269,397,116,129,282

Fig. 4. Reordering array for interleaving in Downlink TDMA6-641-NEW baseline.

Modulation and Slot format

After interleaving across 2 slots the 399 bits are mapped to 8–PSK symbols using the Gray mapping shown in figure 5 (the least significant bit is the right most bit). The bits are mapped in the order shown in Fig. 4 to the timeslot bit order shown in Fig. 6. For example, the first three bits in Row 0 of Fig. 4 are mapped to the first three Data bits in Fig. 6, the next three bits in Row 0 of Fig. 4 are mapped to the next three Data bits in Fig. 6, etc.. This produces 133 complex. All fields represent bits, with the exception of Sync constituted by 14 symbols. Thus, we have F (1 bit) for downlink power control; RSVD (2 bits) reserved bits; PLT (36 bits) for pilot symbols; Data (399 bits); R (6 bits) for ramp time.

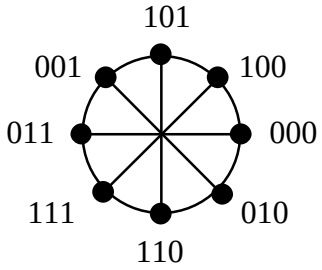

Fig. 5. Gray mapping.

SYNC	F	RSVD	DATA	PLT	DATA	PLT	DATA	PLT	DATA	PLT	R
14 symb	1	2	102	9	99	9	99	9	99	9	6

Fig. 6. Downlink slot format for TDMA6-641 baseline

Performance results

Simulations on 10,000 frames of data were performed to collect class 1A FER-BER, class 1B BER, class 2 BER, and modem BER statistics for the coding scheme discussed above at Doppler frequencies of 10 Hz and 184 Hz , with an ideal coherent 8-PSK receiver. Error statistics reported in the following figures are only for user 1. Error statistics for user 2 are basically the same of user 1. Each plot contains several curves that are explained below:

FER-C1A – Frame error rate for class 1A, detected with CRC failure and with ideal coherent detection.
BER-C1A – User 1 class 1A bit error rate, with ideal coherent detection.
BER-C1B – User 1 class 1B bit error rate, with ideal coherent detection.
BER-C2 – User 1 class 2 bit error rate, with ideal coherent detection.
BER-MOD – User 1 and 2 modem (C1A, C1B, C2 before convolutional decoding) bit error rate, with ideal coherent detection.

It should be noted that TDMA6-641-NEW mainly differs from [1] by using 2 separate CRC, by coding each user independently, and finally by performing scrambling only after coding. As a result of an increased number of CRC bits per slot, we use a rate 3/4 code on class 1B instead of a rate 20/29 code as in [1]. From figures 7 and 8 it can be seen that this modified downlink TDMA6-641 achieves similar performance to the scheme presented in [1].

References

[1] - “TDMA6-641 downlink baseline definition”, Lucent, UWCC.GTF.136+/98.08.12, Toronto.
[2] - “Half rate codec requirements version 1.8”, Lucent, UWCC.GTF.136+/98.11.12.05, San Diego.
[3] - “CRC Requirements”, Lucent, UWCC.GTF.136+/98.09.28.

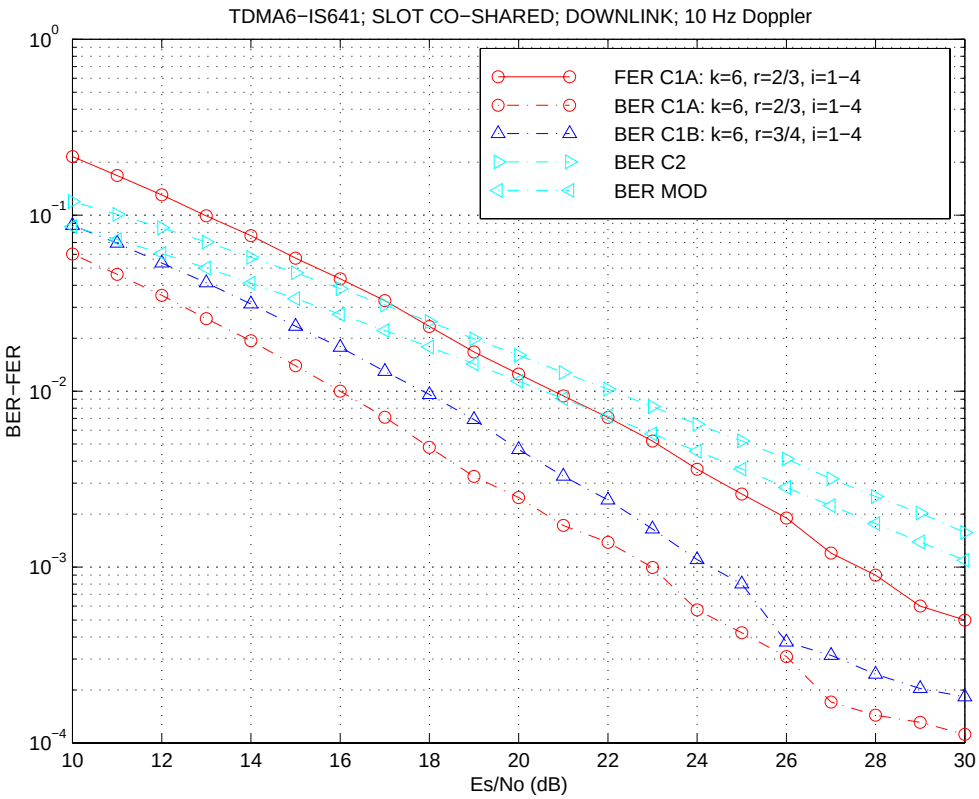

Fig. 7: TDMA6-641-NEW downlink performance at 10 Hz Doppler.

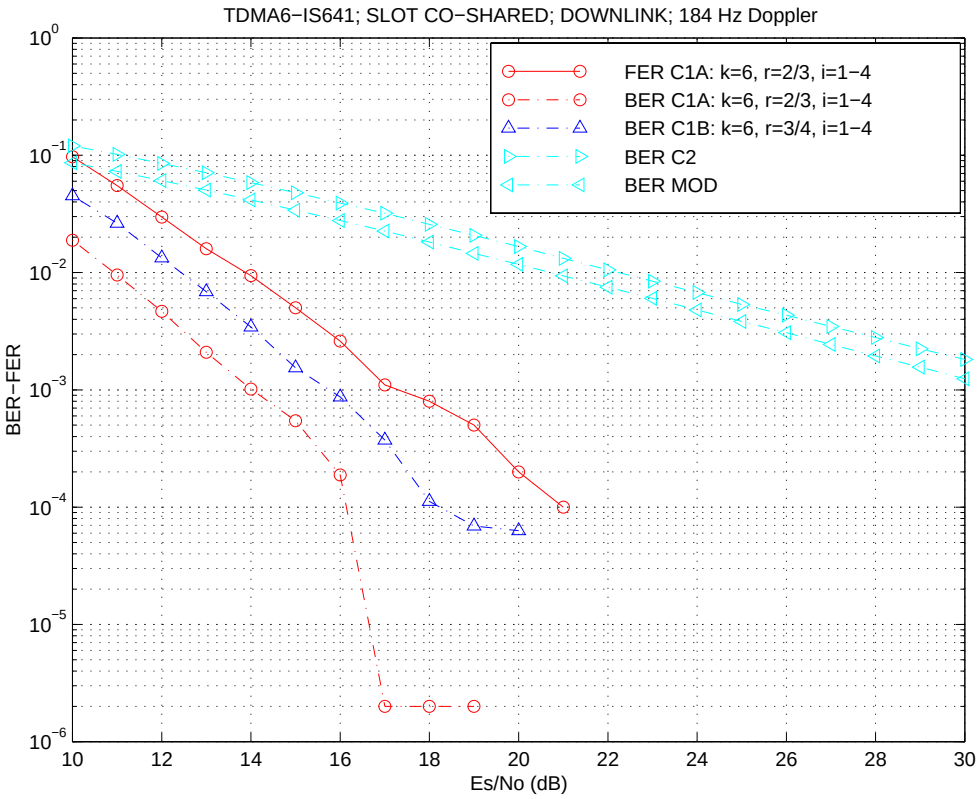

Fig. 8: TDMA6-641-NEW downlink performance at 184 Hz Doppler.