### Title:

TDMA6-641 UPLINK baseline definition.

### Source:

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# Abstract:

In this contribution we propose a baseline scheme for the Uplink TDMA Half Rate mode with IS-641 Acelp (i.e. TDMA6-641). Bits partitions, channel encoding, modulation/mapping, and slot format are addressed and defined. Error performance curves from simulations are shown for both 1 branch and 2 branch antenna diversity. Based on the results here presented, we propose this scheme to be adopted as the baseline definition of TDMA6-641 Uplink.

## **Recommendation:**

Review and adopt the K=6, 2-Branch performance results as a baseline for the TDMA6-641 uplink performance and change the minimum performance criteria for the uplink case to include the effects of diversity.

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#### Introduction

In the following sections we describe our proposal for the definition of the Uplink TDMA Half rate mode with IS-641 Acelp vocoder. We refer to the Half Rate mode using IS-641 Acelp codec as TDMA6-641. Since in the Half Rate mode we have to support 6 simultaneous voice calls, each user can be only assigned to one slot inside the 40 ms TDMA frame. For instance, user 1 is allocated to slot number 1. Since one slot interleaving translates in poor performance, it is needed to provide inter-slot interleaving in a fashion similar to the defined IS-136 Full Rate mode. It should be noted that while in IS-136 Full Rate it is possible to implement inter-slot interleaving among slots number 1 and 4 (since they belong to the same user), in the Uplink Half Rate mode inter-slot interleaving can only be accomplished among slots number 1 of adjacent frames (fig.1). We refer to this 2 inter-slot interleaving scheme as 1-7 interleaving scheme.



Fig. 1: Frame format and slot allocation to user 1 in TDMA6 Uplink.

#### Bits partition at the Acelp vocoder output

As we said, each TDMA6-641 user transmits his information every 40 ms. This means, that now we need a speech buffer of length 40 ms. Since Acelp rate is 7.4 kb/s, in 40 ms the codec outputs 296 bits. We partition these bits in 96 class 1A, 96 class 1B, and 104 class 2 bits.

#### **Channel encoding**

We choose to protect the class 1A bits with 8 bits CRC, then we encode the 96 class 1A bits plus 8 bits of CRC with a tail biting convolutional code with constraint length K=6 or 7, rate 7/10. Thus we obtain 148 total class 1A coded bits. Class 1B are still protected with a tail biting convolutional code with constraint length K=6 or 7, but with rate 4/5. This produces 120 coded class 1B bits. These codes are obtained from a punctured rate  $\frac{1}{2}$  mother code. Code polynomials are shown in figure 2, while puncturing matrixes are shown in figure 3. Class 2 bits are left uncoded. Finally the total number of bits at the output of the convolutional encoder (i.e. coded class 1A + coded CRC+ coded class 1B + class 2) is 372.

 $G_{k=6}=[075 \ 053]$   $G_{k=7}=[0133 \ 0171]$ 

**Fig. 2.** Polynomials for K=6 and K=7, in octal representation.

Class 1A:  $\begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 0 & 0 & 1 \end{bmatrix}$  Class 1B:  $\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 \end{bmatrix}$ 

Fig. 3. Puncturing matrices for class 1A and class 1B bits.

### **Reordering and Interleaving**

After encoding, the bits are arranged in priority order format (class 1 followed by class 2). The resulting vector of 372 bits is indexed from 0 to 371 and reordered using the matrix given in figure 4. Bits from 0 to 147 are coded class 1A + CRC, bits from 148 to 267 are coded class 2, and finally bits from 260 to 371 are class 2. Inter-slot interleaving can now be accomplished simply transmitting in each time slot half of the bits that belong to the current speech frame and half the bits that belong to the previous speech frame. After reordering the bits, the odd-indexed rows (1,3,...,15) are exchanged with the corresponding rows from the next speech frame. Thus, the even indexed rows (0,2,...,14) are kept within the same slot, e.g. slot 1, but the odd-indexed rows are placed in slot 1 of the next 40 ms frame.

Row 0	0,148,268,16,164,284,32,180,300,48,196,316,64,212,332,80,228,348,96,244,260,112,124,136,
Row 1	1,149,269,17,165,285,33,181,301,49,197,317,65,213,333,81,229,349,97,245,261,113,125,137,
Row 2	2,150,270,18,166,286,34,182,302,50,198,318,66,214,334,82,230,350,98,246,262,114,126,138,
Row 3	3,151,271,19,167,287,35,183,303,51,199,319,67,215,335,83,231,351,99,247,263,115,127,139,
Row 4	4,152,272,20,168,288,36,184,304,52,200,320,68,216,336,84,232,352,100,248,264,116,128,140,
Row 5	5,153,273,21,169,289,37,185,305,53,201,321,69,217,337,85,233,353,101,249,265,117,129,141,
Row 6	6,154,274,22,170,290,38,186,306,54,202,322,70,218,338,86,234,354,102,250,266,118,130,142,
Row 7	7,155,275,23,171,291,39,187,307,55,203,323,71,219,339,87,235,355,103,251,267,119,131,143,
Row 8	8,156,276,24,172,292,40,188,308,56,204,324,72,220,340,88,236,356,104,252,364,120,132,144,
Row 9	9,157,277,25,173,293,41,189,309,57,205,325,73,221,341,89,237,357,105,253,365,121,133,145,
Row 10	10,158,278,26,174,294,42,190,310,58,206,326,74,222,342,90,238,358,106,254,366,122,134,146,
Row 11	11,159,279,27,175,295,43,191,311,59,207,327,75,223,343,91,239,359,107,255,367,123,135,147,
Row 12	12,160,280,28,176,296,44,192,312,60,208,328,76,224,344,92,240,360,108,256,368,
Row 13	13,161,281,29,177,297,45,193,313,61,209,329,77,225,345,93,241,361,109,257,369,
Row 14	14,162,282,30,178,298,46,194,314,62,210,330,78,226,346,94,242,362,110,258,370,
Row 15	15,163,283,31,179,299,47,195,315,63,211,331,79,227,347,95,243,363,111,259,371

Fig. 4. Reordering array for interleaving in Uplink TDMA6-641 baseline.

This interleaving scheme introduces the following delay:

40 ms (buffering) + 40 ms (interleaving) + 6.67 ms (transmission) = 86.67 ms

#### **Modulation and Slot format**

After interleaving across 2 slots the 372 bits are mapped to 8–PSK symbols using the Gray mapping shown in figure 5 (the least significant bit is the right most bit). This produces 124 complex symbols that are placed in the slot data fields as shown in figure 6. All fields represent bits, with the exception of the Sync field that represents 14 symbols. Thus, we have G (9 bits) for guard time; R (9 bits) for ramp time; FPC, 1 bit for power control, plus 2 reserved bits; PLT (27 bits) for plot symbols; Data (372 bits); Sacch (12 bits) for the slow associated control channel; Cdvcc (12 bits) for the coded digital verification color code.



Fig. 5. Gray mapping.

G	R	Plt	Fpc	Data	Sync	Sacch	Data	Plt	Data	Cdvcc	Data	Plt
9	9	9	3	96	14 s	12	90	9	90	12	96	9

Fig. 6. Uplink slot format for TDMA6-641 baseline

#### **Performance results**

Simulations on 10,000 frames of data were performed to collect class 1A FER-BER, class 1B BER, class 2 BER, and modem BER statistics for the coding schemes discussed above at Doppler frequencies of 10 Hz

and 184 Hz. Figs. 7 and 9 show the performance curves at 10 Hz Doppler with K=6 and K=7 respectively, obtained with an ideal 8-PSK receiver with no antenna diversity. Fig. 8 and 10 report performance curves at 184 Hz Doppler for K=6 and K=7 respectively, obtained with an ideal 8-PSK receiver with no antenna diversity. Figures 11-14 report performance curves obtained with an ideal 8-PSK receiver when 2 branch antenna diversity is deployed. Each plot contains several curves that are explained below:

- **FER-C1A** Frame error rate for class 1A, detected with CRC failure and with ideal coherent detection.
- **BER-C1A** Bit error rate for class 1A, with ideal coherent detection.
- **BER-C1B** Bit error rate for class 1B, with ideal coherent detection.
- **BER-C2** Bit error rate for class 2, with ideal coherent detection.
- **BER-MOD** Bit error rate for modem bits, with ideal coherent detection.

We report the list of figures in the following:

Fig. 7:	1 BRANCH, 10 Hz Doppler, K=6.
Fig. 8:	1 BRANCH, 184 Hz Doppler, K=6.
Fig. 9:	1 BRANCH, 10 Hz Doppler, K=7.
Fig. 10:	1 BRANCH, 184 Hz Doppler, K=7.
Fig. 11:	2 BRANCH, 10 Hz Doppler, K=6.
Fig. 12:	2 BRANCH, 184 Hz Doppler, K=6.
Fig. 13:	2 BRANCH, 10 Hz Doppler, K=7.
Fig. 14:	2 BRANCH, 184 Hz Doppler, K=7.

In order determine the best baseline curve for the uplink minimum performance specification, we need to compare the results in Figs. 7-14 to the performance of Full-Rate IS-641 under the same conditions. Simulations of Full-Rate IS-641 have been performed and Table 1 summarizes the results for C1A FER with K=6 at 1%. The Full Rate IS-641 results have been obtained with an ideal receiver for pi/4 DQPSK (i.e. a receiver that requires perfect knowledge of channel state information).

	Doppler (Hz)	IS-641	TDMA6-641	Delta			
No Diversity	10	16.3 dB	22 dB	5.7 dB			
No Diversity	184	10.8 dB	15.2 dB	4.4 dB			
2-Branch Diversity	10	8.2 dB	11.5 dB	3.3 dB			
2-Branch Diversity	184	4.8 dB	8.3 dB	3.5 dB			

**Table 1.** Es/No required to obtain 1% C1A FER with K=6.

Note that the difference between IS-641 and TDMA6-641 with no diversity on the uplink is about 6 dB at 10 Hz. However, the difference between IS-641 and TDMA6-641 with diversity on the uplink is only about 3.5 dB at 10 Hz. This shows that there is a much smaller difference in performance between IS-641 and TDMA6-641 when 2-branch diversity is present. Since uplink 2-branch diversity is commonly present in almost every cell site, the above data indicates that basing the uplink minimum performance criteria for the uplink should require that the HR vocoder provide voice quality in the presence of background noise that is equivalent to or greater than the better of IS-641 with diversity at 8.2 dB C/N, IS-641 with diversity at x-4 dB and TDMA6-641 with diversity at x dB.



TDMA6-IS641; UPLINK; 10 Hz Doppler



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TDMA6-IS641; UPLINK; 10 Hz Doppler



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Fig. 11: 2 Branch diversity performance curves at 10 Hz Doppler with K=6.

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Fig. 12: 2 Branch diversity performance curves at 184 Hz Doppler with K=6.

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**Fig. 13:** 2 Branch diversity performance curves at 10 Hz Doppler with K=7.

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Fig. 14: 2 Branch diversity performance curves at 184 Hz Doppler with K=7.