Title:

TDMA6-641 DOWNLINK baseline definition.

Source:

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Abstract:

In this contribution we describe a baseline scheme for the Downlink TDMA Half Rate mode with IS-641 Acelp (i.e. TDMA6-641). This contribution follows [1], and has improved channel coding scheme, and interleaving scheme. Bits partitions, channel encoding, modulation/mapping, and slot format are addressed and defined. Error performance curves from simulations are shown.

Recommendation:

Review and adopt.

Introduction

In the following sections we describe a proposal for the definition of the Downlink TDMA Half rate mode with IS-641 Acelp vocoder. We refer to the Half Rate mode using IS-641 Acelp codec as TDMA6-641. In the Half Rate mode we have to support 6 simultaneous voice calls. In order to achieve good interleaving gains and keeping the delay small we share the information of two users in one slot. For instance, user 1 and 2 are allocated to slot number 1 and 4 (figure 1). Furthermore, the information bits of user 1 and user 2 are uniformly distributed in each slot. This is done in order to obtain the highest amount of time diversity inside a slot, and equally to both users sharing the same slot. Then inter-slot interleaving (between slots 1 and 4) is implemented in a fashion similar to the one defined IS-136 Full Rate mode. We refer to this 2 inter-slot interleaving scheme with two users sharing the same slot, as 1-4 slot co-shared interleaving scheme.

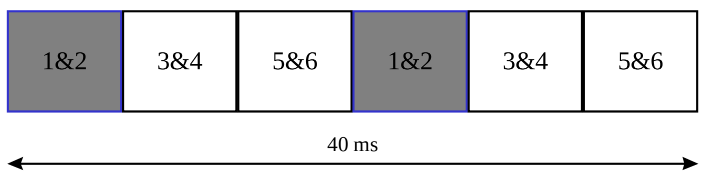

Fig. 1: Frame format and slot allocation to users in TDMA6 Downlink with slot co-sharing among pair of users.

Bits partition at the Acelp vocoder output

In the downlink, each TDMA6-641 user transmits his information every 20 ms. This means, that we need a speech buffer of length 20 ms. Since Acelp rate is 7.4 kb/s, in 20 ms the codec outputs 148 bits. We partition these bits in 48 class 1A, 48 class 1B, and 52 class 2 bits. Since now we share the information of 2 users, two speech buffers of 20 ms are concatenated. In other words, the total amount of bits from 2 users in 20 ms is 296 : 96 class 1A, 96 class 1B and 104 class 2.

Scrambling

Before encoding, the bits of the 2 users are scrambled. In particular, class 1A bits of user 1 are scrambled with class 1A bits of user 2; class 1B bits of user 1 are scrambled with class 1B bits of user 2; class 2 bits of user 1 are scrambled with class 2 bits of user 2. Thus, indicating with *a1* the 48 class1 A bits of user 1, with *a2* the 48 bits of user 2, then the 96 scrambled bits of class 1A are *bC1A*:

$$bC1A(2i) = a1(i), \qquad i = 0,1,\ldots,47$$

$$bC1A(2i+1) = a2(i), \qquad i = 0,1,\ldots,47$$

Similarly, indicating with *b1* the 48 class1 B bits of user 1, with *b2* the 48 bits of user 2, then the 96 scrambled bits of class 1B are *bC1B*:

$$bC1B(2i) = b1(i), \qquad i = 0,1,\ldots,47$$

$$bC1B(2i+1) = b2(i), \qquad i = 0,1,\ldots,47$$

Finally indicating with *c1* the 52 class2 bits of user 1, with *c2* the 52 bits of user 2, the 104 scrambled bits of class 2 are *bC2* :

$$bC2(2i) = c1(i), \qquad i = 0,1,\ldots,51$$

$$bC2(2i+1) = c2(i), \qquad i = 0,1,\ldots,51$$

Channel encoding

We choose to add to class 1A bits, *bC1A(i)* , 8 bits of CRC. Then we encode the 96 class 1A bits plus 8 bits of CRC with a tail biting convolutional code with constraint length K=6 or 7, rate 2/3. Thus we obtain 156 total class 1A coded bits. Class 1B, *bC1B(i),* are still protected with a tail biting convolutional code with constraint length K=6 or 7, but with rate 20/29. This produces 139 coded class 1B bits. These codes are obtained from a punctured rate ½ mother code. Code polynomials are shown in figure 2, while puncturing matrixes are shown in figure 3. Class 2 bits are left uncoded. Finally the total number of bits at the output of the convolutional encoder (i.e. coded class 1A + coded CRC+ coded class 1B + class 2) is 399.

$$G_{k=6}=[\ 075 \quad 053\ ] \qquad G_{k=7}=[\ 0133 \ \ 0171\ ]$$

Fig. 2. Polynomials for K=6 and K=7, in octal representation.

$$\text{Class 1A: } \begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix}$$

$$\text{Class 1B: } \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

Fig. 3. Puncturing matrices for class 1A and class 1B bits.

Reordering and Interleaving

After encoding, the bits are arranged in priority order format (class 1 followed by class 2). The resulting vector of 399 bits is indexed from 0 to 398 and reordered using the matrix given in figure 4. Bits from 0 to 155 are coded class 1A + CRC, bits from 156 to 295 are coded class 2, and finally bits from 296 to 398 are class 2. Inter-slot interleaving can now be accomplished simply transmitting in each time slot half of the bits that belong to the current speech frame and half the bits that belong to the previous speech frame. After reordering the bits, the odd-indexed rows (1,3,…,13) are exchanged with the corresponding rows from the next speech frame. Thus, the even indexed rows (0,2,…,12) are kept within the same slot, e.g. slot 1, but the odd-indexed (1,3,...,13) rows are placed in slot 4 of the next 20 ms frame.

Row 0	0,156,295,13,169,308,26 ,182,321,39 ,195,334,52,208,347,65,221,360,78,234,373,91 ,247,386, 104,117,260,130,136,273,142,147,152,280,285,290,
Row 1	1,157,296,14,170,309,27 ,183,322,40 ,196,335,53,209,348,66,222,361,79,235,374,92 ,248,387, 105,118,261,131,137,274,143,148,153,281,286,291,
Row 2	2,158,297,15,171,310,28 ,184,323,41 ,197,336,54,210,349,67,223,362,80,236,375,93 ,249,388, 106,119,262,132,138,275,144,149,154,282,287,292,
Row 3	3,159,298,16,172,311,29 ,185,324,42 ,198,337,55,211,350,68,224,363,81,237,376,94 ,250,389, 107,120,263,133,139,276,145,150,155,283,288,293,
Row 4	4,160,299,17,173,312,30 ,186,325,43 ,199,338,56,212,351,69,225,364,82,238,377,95 ,251,390, 108,121,264,134,140,277,146,151,279,284,289,294,
Row 5	5,161,300,18,174,313,31 ,187,326,44 ,200,339,57,213,352,70,226,365,83,239,378,96 ,252,391, 109,122,265,135,141,278,
Row 6	6,162,301,19,175,314,32 ,188,327,45 ,201,340,58,214,353,71,227,366,84,240,379,97 ,253,392, 110,123,266,
Row 7	7,163,302,20,176,315,33 ,189,328,46 ,202,341,59,215,354,72,228,367,85,241,380,98 ,254,393, 111,124,267,
Row 8	8,164,303,21,177,316,34 ,190,329,47 ,203,342,60,216,355,73,229,368,86,242,381,99 ,255,394, 112,125,268,
Row 9	9,165,304,22,178,317,35 ,191,330,48,204,343,61,217,356,74,230,369,87,243,382,100,256,395, 113,126,269,
Row 10	10,166,305,23,179,318,36 ,192,331,49 ,205,344,62,218,357,75,231,370,88,244,383,101,257,396, 114,127,270,
Row 11	11,167,306,24,180,319,37 ,193,332,50 ,206,345,63,219,358,76,232,371,89,245,384,102,258,397, 115,128,271,
Row 12	12,168,307,25,181,320,38 ,194,333,51 ,207,346,
Row 13	64,220,359,77,233,372,90 ,246,385,103,259,398,116,129,272

Fig. 4. Reordering array for interleaving in Downlink TDMA6-641 baseline.

This interleaving scheme introduces the following delay: 20 ms (buffering) + 20 ms (interleaving) + 6.67 ms (transmission)=46.67 ms

Modulation and Slot format

After interleaving across 2 slots the 399 bits are mapped to 8−PSK symbols using the Gray mapping shown in figure 5 (the least significant bit is the right most bit). This produces 133 complex symbols that are placed in the slot data fields as shown in figure 6. All fields represent bits, with the exception of Sync constituted by 14 symbols. Thus, we have F (1 bit) for downlink power control; RSVD (2 bits) reserved bits; PLT (36 bits) for pilot symbols; Data (399 bits); R (6 bits) for ramp time.

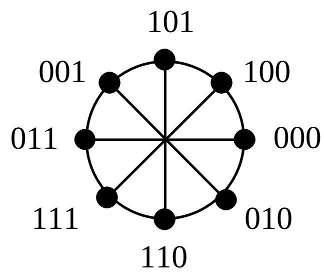

Fig. 5. Gray mapping.

SYNC 14 symb	F 1	RSVD 2	DATA 102	PLT 9	DATA 99	PLT 9	DATA 99	PLT 9	DATA 99	PLT 9	R 6

Fig. 6. Downlink slot format for TDMA6-641 baseline

Performance results

Simulations on 10,000 frames of data were performed to collect class 1A FER-BER, class 1B BER, class 2 BER, and modem BER statistics for the coding schemes discussed above at Doppler frequencies of 10 Hz and 184 Hz. Error statistics reported in the following figures are only for user 1. This is because error statistics for user 2 have been investigated, and they were the same as for user 1, as a result of the uniformly distribution of the 2 users bits along the same slot. However, it should be noted that since we add 8 bit of CRC to the scrambled class 1A bits, then a CRC failure indicates that one or both users have at least one class 1A bit in error. Further investigations (here not reported) have shown that C1A FER detected with CRC equals in average the C1A FER of user 1 ideally detected. Figs. 7 and 9 show the performance curves at 10 Hz Doppler with K=6 and K=7 respectively, with an ideal coherent 8-PSK receiver. Fig. 8 and 10 report performance curves at 184 Hz Doppler for K=6 and K=7 respectively, with an ideal coherent 8-PSK receiver. Each plot contains several curves that are explained below:

FER-C1A – Frame error rate for class 1A, detected with CRC failure and with ideal coherent detection.
BER-C1A – User 1 class 1A bit error rate, with ideal coherent detection.
BER-C1B – User 1 class 1B bit error rate, with ideal coherent detection.
BER-C2 **–** User 1 class 2B bit error rate, with ideal coherent detection.
BER-MOD **–** User 1 and 2 modem (C1A, C1B, C2 before convolutional decoding) bit error rate, with ideal coherent detection.

References

[1] **-** “Downlink TDMA6-641 performance curves”, Lucent, UWCC.GTF.136+/98.06.22

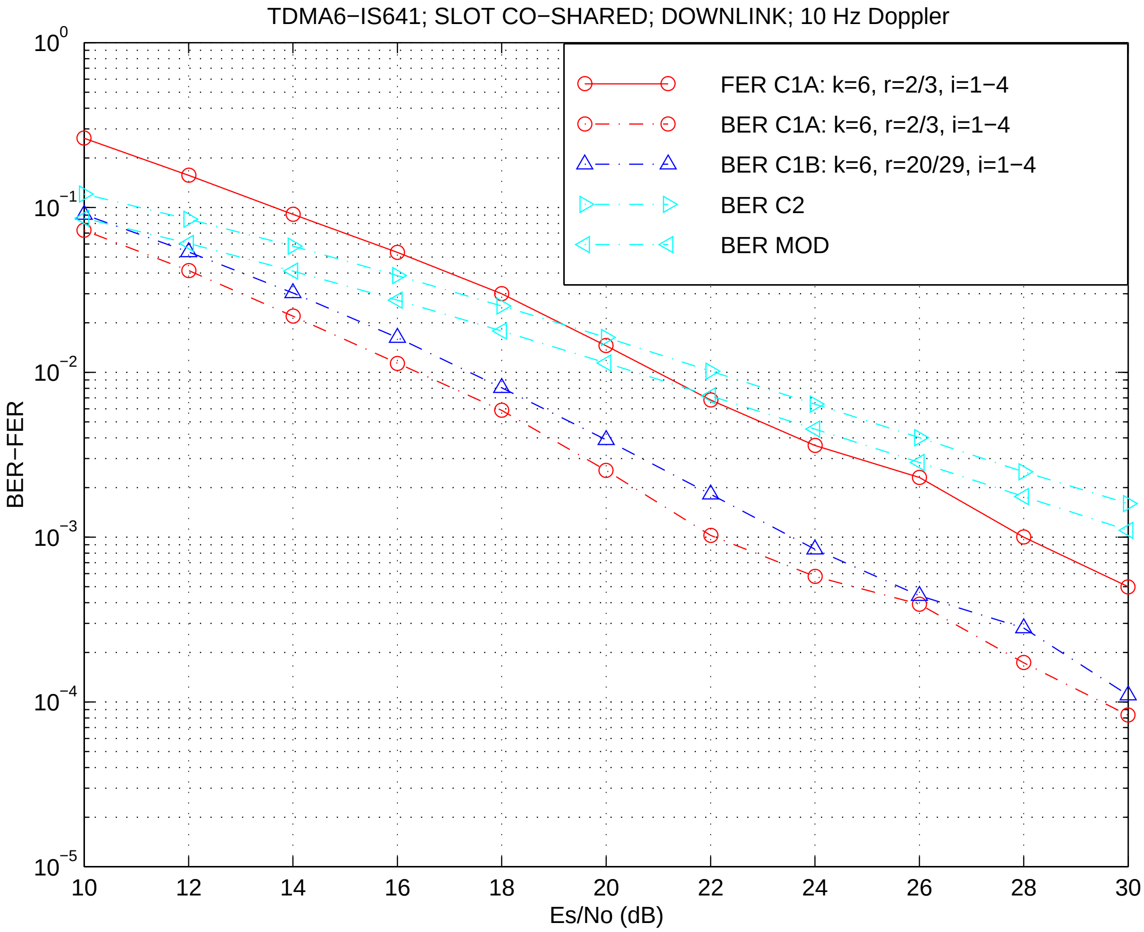

Fig. 7: TDMA6-641 downlink performance at 10 Hz Doppler. User 1 with slot co-shared with user 2 and constraint length K=6.

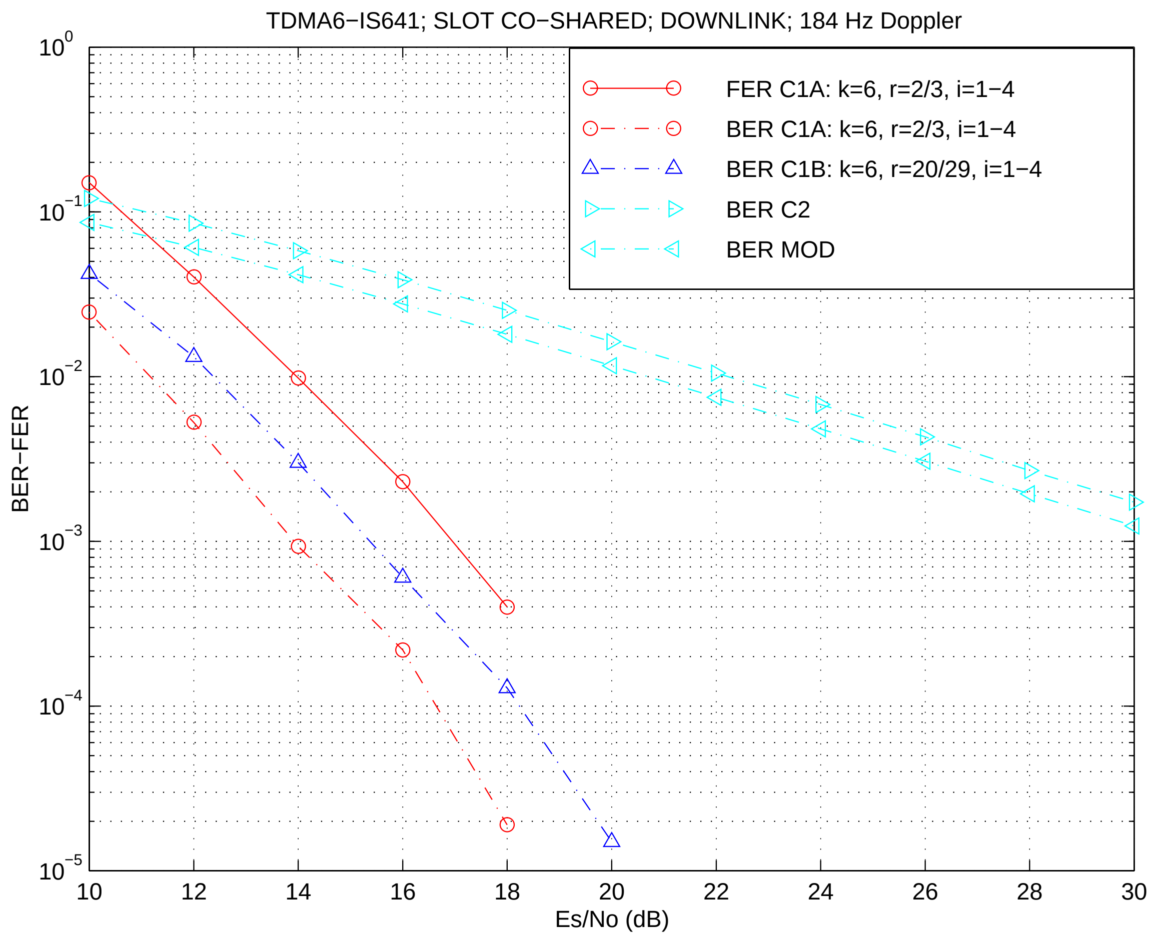

Fig. 8: TDMA6-641 downlink performance at 184 Hz Doppler. User 1, with slot co-shared with user 2 and constraint length K=6.

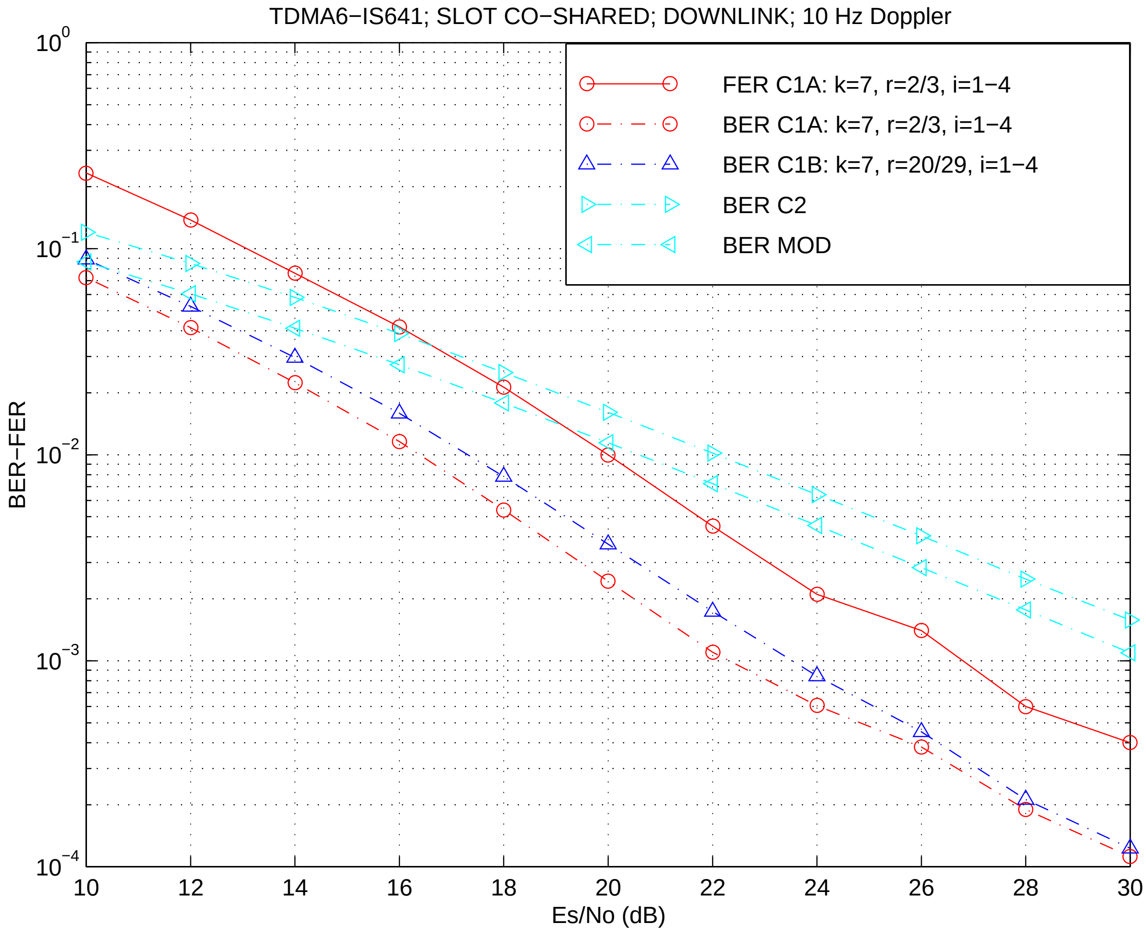

Fig. 9: TDMA6-641 downlink performance at 10 Hz Doppler. User 1, with slot co-shared with user 2 and constraint length K=7.

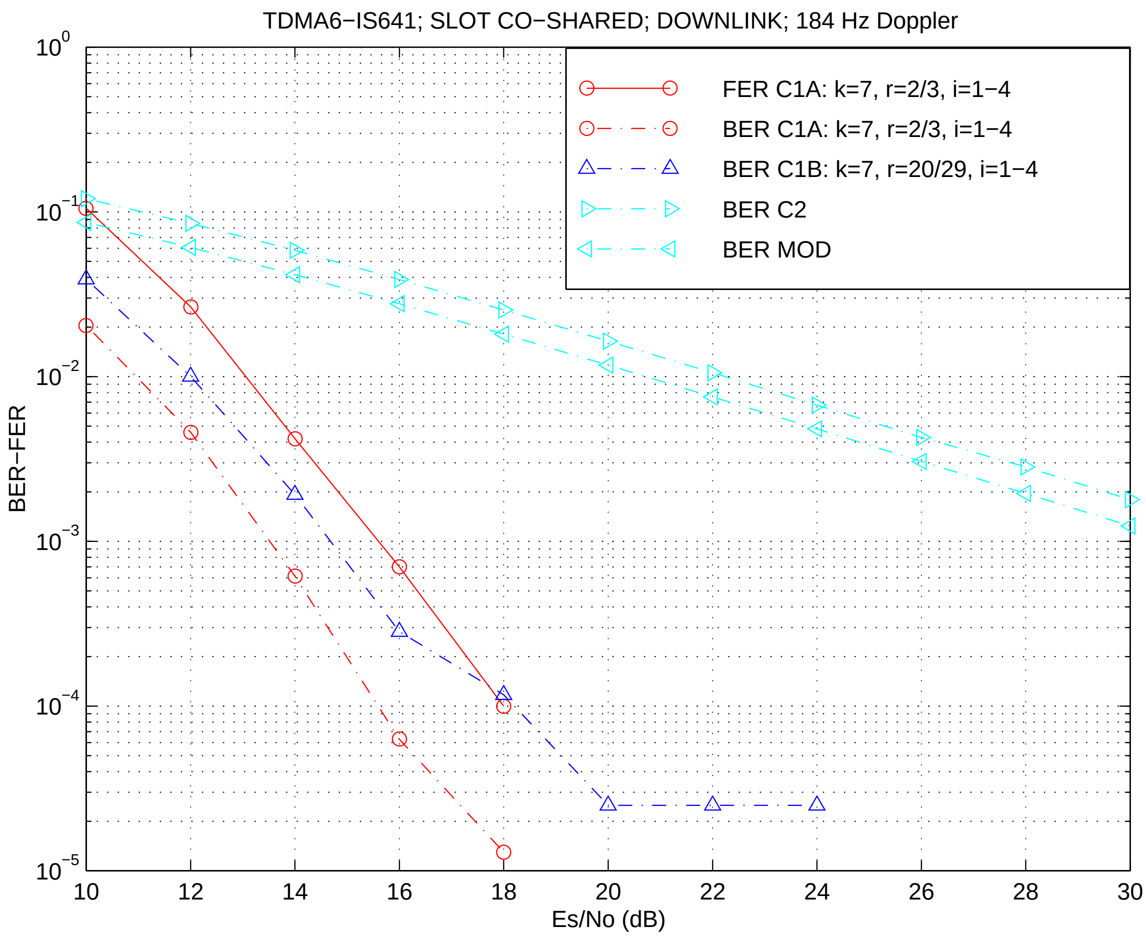

Fig. 10: TDMA6-641 downlink performance at 184 Hz Doppler. User 1, with slot co-shared with user 2 and constraint length K=7.