Title:

New Channel Coding with New Slot Format for the IS-641 Codec Using π/4-DQPSK.

Source:

James P. Seymour	Srinivas R. Kadaba	Andrea M. Tonello
Lucent Technologies	Lucent Technologies	Lucent Technologies
Network Wireless Systems	Network Wireless Systems	Network Wireless Systems
67 Whippany Rd. Rm. 14A331	67 Whippany Rd. Rm. 14A331	67 Whippany Rd. Rm. 1A210
(973)-386-8096 (v)	(973)-581-6861 (v)	(973)-386-5192 (v)
(973)-386-6814 (f)	(973)-386-2651 (f)	(973)-386-2651 (f)
jpseymour@lucent.com	skadaba@lucent.com	tonello@lucent.com

Abstract:

This contribution provides performance results of simulations of a particular channel coding scheme for the IS-641 codec which can be used over a new π/4-DQPSK timeslot format which takes advantage of the removal of the SACCH and CDL data fields. The DVCC, ramp and FPC fields are still maintained for equalization and downlink power control purposes. Results show that this scheme can improve the Class 1A FER by 2 dB while at the same time improve the Class 1B BER slightly compared to the current IS-641 channel coding scheme.

Recommendation:

Review and adopt.

Notices:

Introduction

This contribution presents a new channel coding and interleaving scheme for the IS-641 codec for IS-136+ which takes advantage of a new timeslot format which eliminates the SACCH and CDL data fields. The removal of the SACCH and CDL fields has been studied in [1] and [2]. The new timeslot format maintains the DVCC field for equalization purposes and also includes 3 symbols for ramp and FPC signaling for downlink power control purposes. The new scheme proposed here will be referred to as IS-641+ to differentiate it from the existing IS-641 scheme for IS-136. Error rate performance curves are presented for IS-641+ and are compared with those of IS-641 at Doppler frequencies of 10, 60, and 170 Hz. For the purposes of this contribution, the demodulation scheme used for both the IS-641 and IS-641+ simulations was differential detection. The same improvement is expected if a more advanced detection scheme using channel phase estimates was used for both IS-641 and IS-641+.

Simulation Details

Channel Encoding

The IS-641+ speech frame consists of 48 Class 1A, 48 Class 1B and 52 Class 2 bits. The Class 1A bits are protected by a 7-bit CRC. The 48 Class 1A and 7 CRC bits are encoded using a rate 2/5 convolutional code (punctured rate 1/3 code). Fig. 1 shows the puncturing matrix used for the Class 1A bits. This produces 137 coded bits. The Class 1B bits are encoded using a rate 7/13 convolutional code (punctured rate ½ code). Figure 1 also shows the puncturing matrix for the Class 1B bits. This produces another 89 coded bits. Thus, the encoding process produces 226 coded bits. Combining these with the 52 Class 2 bits yields 278 total data bits used for speech. Adding to this 28 bits for Sync and 12 bits for CDVCC results in 318 total bits. This leaves 6 bits (or 3 symbols) for FPC signaling and ramp symbols for downlink power control. Figure 2 summarizes the encoding scheme. Constraint lengths of K=6 and K=7 were simulated for both codes.

Class 1A

1	1
1	1
0	1

Class 1B

1	1	1	1	1	1	1
0	1	1	1	1	1	1

Figure 1. Puncturing matrices for Class 1A and Class 1B bits.

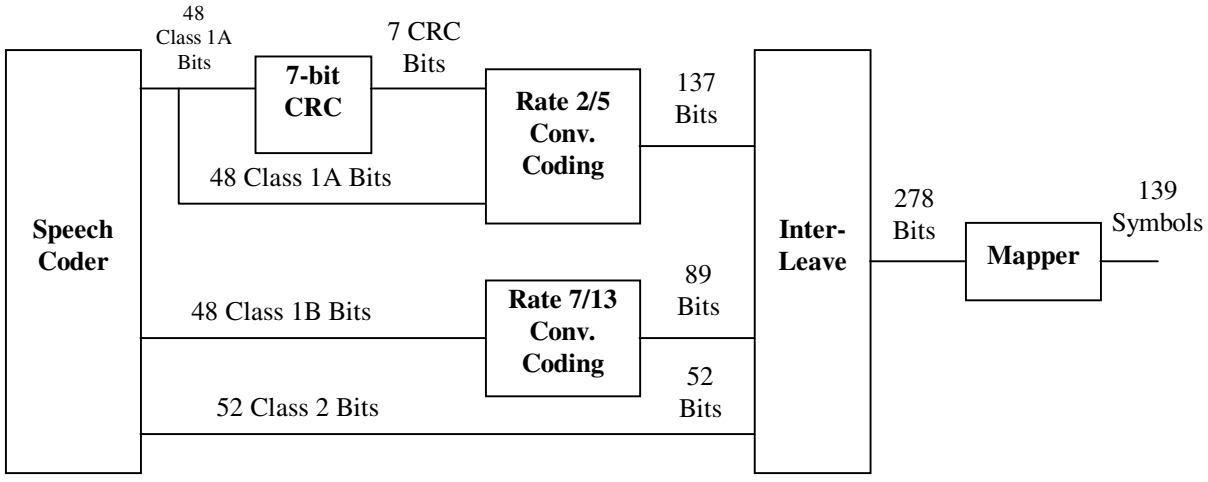

Figure 2. IS-641+ π/4-DQPSK Channel Coding.

Reordering
After encoding, the bits are arranged in priority order format (Class 1 followed by Class 2). The resulting vector of 278 bits is indexed from 0 to 277 and reordered using the following matrix:

Table 1. Reordering Matrix for Interleaving.

Row 0	220	219	218	233	232	231	211	210	209	208
Row 1	0	27	54	81	108	135	162	189	223	253
Row 2	1	28	55	82	109	136	163	190	224	254
Row 3	2	29	56	83	110	137	164	191	225	255
Row 4	3	30	57	84	111	138	165	192	226	256
Row 5	4	31	58	85	112	139	166	193	227	257
Row 6	5	32	59	86	113	140	167	194	228	258
Row 7	6	33	60	87	114	141	168	195	229	259
Row 8	7	34	61	88	115	142	169	196	230	260
Row 9	8	35	62	89	116	143	170	197	234	261
Row 10	9	36	63	90	117	144	171	198	235	262
Row 11	10	37	64	91	118	145	172	199	236	263
Row 12	11	38	65	92	119	146	173	200	237	264
Row 13	12	39	66	93	120	147	174	201	238	265
Row 14	13	40	67	94	121	148	175	202	239	266
Row 15	14	41	68	95	122	149	176	203	240	267
Row 16	15	42	69	96	123	150	177	204	241	268
Row 17	16	43	70	97	124	151	178	205	242	269
Row 18	17	44	71	98	125	152	179	206	243	270
Row 19	18	45	72	99	126	153	180	207	244	271
Row 20	19	46	73	100	127	154	181	212	245	272
Row 21	20	47	74	101	128	155	182	213	246	273
Row 22	21	48	75	102	129	156	183	214	247	274
Row 23	22	49	76	103	130	157	184	215	248	275
Row 24	23	50	77	104	131	158	185	216	249	276
Row 25	24	51	78	105	132	159	186	217	250	277
Row 26	25	52	79	106	133	160	187	221	251	
Row 27	26	53	80	107	134	161	188	222	252	

Interslot Interleaving
After reordering the bits as shown above, the odd-indexed rows (1,3,…,27) are exchanged with the corresponding rows from the next speech frame. Thus, the even indexed rows (0,2,…,260) are kept within the same slot, e.g. slot 1, but the odd-indexed rows are placed in the next slot, e.g. slot 4.

Modulation
The data bits are mapped to $\pi/4$-QPSK symbols using a common Gray mapping.

Time Slot Format
The timeslot format used for the IS-641+ simulations is shown below. The current IS-136 timeslot format was used for the IS-641 simulations.

28	140	12	138	6
SYNC	DATA	CDVCC	DATA	FPC/Ramp

Demodulation
Differential detection was used to demodulate the received signals for both the IS-641 and IS-641+ simulations.

Channel Decoding
Viterbi decoding using soft decision metrics as inputs was used to perform the error correction. The decoded Class 1A bits were then used to regenerate the CRC bits which were then compared to the decoded CRC bits. The FER curves presented in the next section show the rate at which frames result in a CRC mismatch. The decoded Class 1B bits were compared to the known Class 1B bits prior to encoding at the transmit end to determine the decoded Class 1B BER curves shown in the next section.

Performance Results

Simulations on 10,000 frames of data were performed to collect FER and Class 1B BER statistics for the coding scheme discussed above at Doppler frequencies of 10, 60 and 170 Hz. Figs. 3 and 4 show the FER and Class 1B BER performance curves of the IS641+ coding scheme for constraint lengths of K=6 and K=7 respectively at a Doppler rate of 10 Hz. In both figures, the performance of the current IS-641 coding scheme using K=6 is shown for comparison purposes. These figures show that the FER using the IS-641+ coding scheme is improved by 1.5 to 2.0 dB, compared to the current IS-641 codec, depending on the constraint length K which is used. Using a K=7 provides approximately 2 dB improvement in FER. At the same time, these figures show that the IS-641+ Class 1B BER is as good or better than the IS-641 Class 1B BER performance. Using a K=7, the IS-641+ Class 1B BER performance is actually about .5 dB better than the IS-641 Class 1B BER performance. Fig. 5 shows the improvement gained in FER and Class 1B BER by going to larger constraint lengths with the IS-641+ coding scheme.

Figs. 6-11 show the same data but at Doppler rates of 60 and 170 Hz. Again it is seen in these figures that a 2 dB improvement in FER is possible with the IS-641+ coding scheme using K=7 compared to the current IS-641 coding scheme. At the same time, the Class 1B BER can be improved by about .5 dB by using a K=7 code. By improving the FER by 2 dB while at the same time improving the Class 1B BER by .5 dB, it is clear that significant coverage improvements can be gained with the current ACELP vocoder, without sacrificing voice quality, by utilizing the suggested channel coding scheme with K=7.

Based on the above discussion, it is recommended that the proposed π/4-DQPSK slot format using the new (IS-641+) channel coding scheme discussed in this contribution with constraint length K=7 be adopted for use with the ACELP vocoder for IS136+.

Figure 3. IS641+ Error Rate Performance at 10 Hz Doppler with K=6.

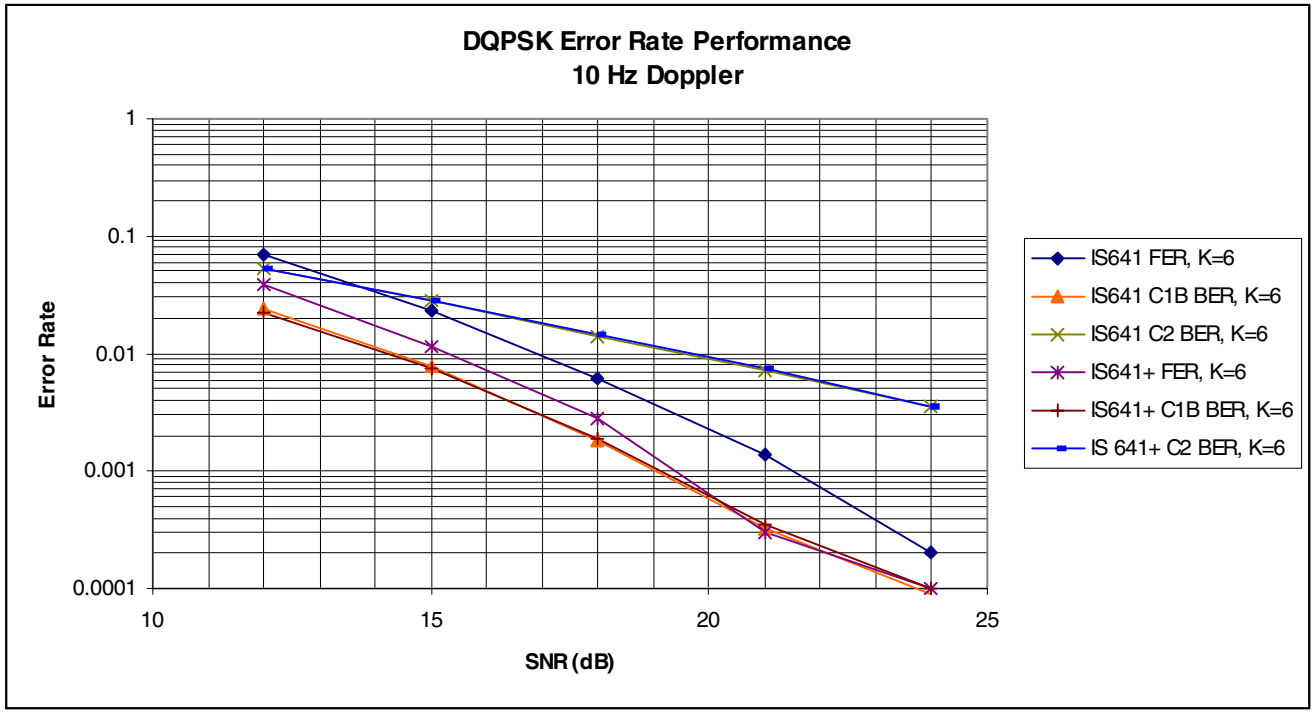

Figure 4. IS641+ Error Rate Performance at 10 Hz Doppler with K=7.

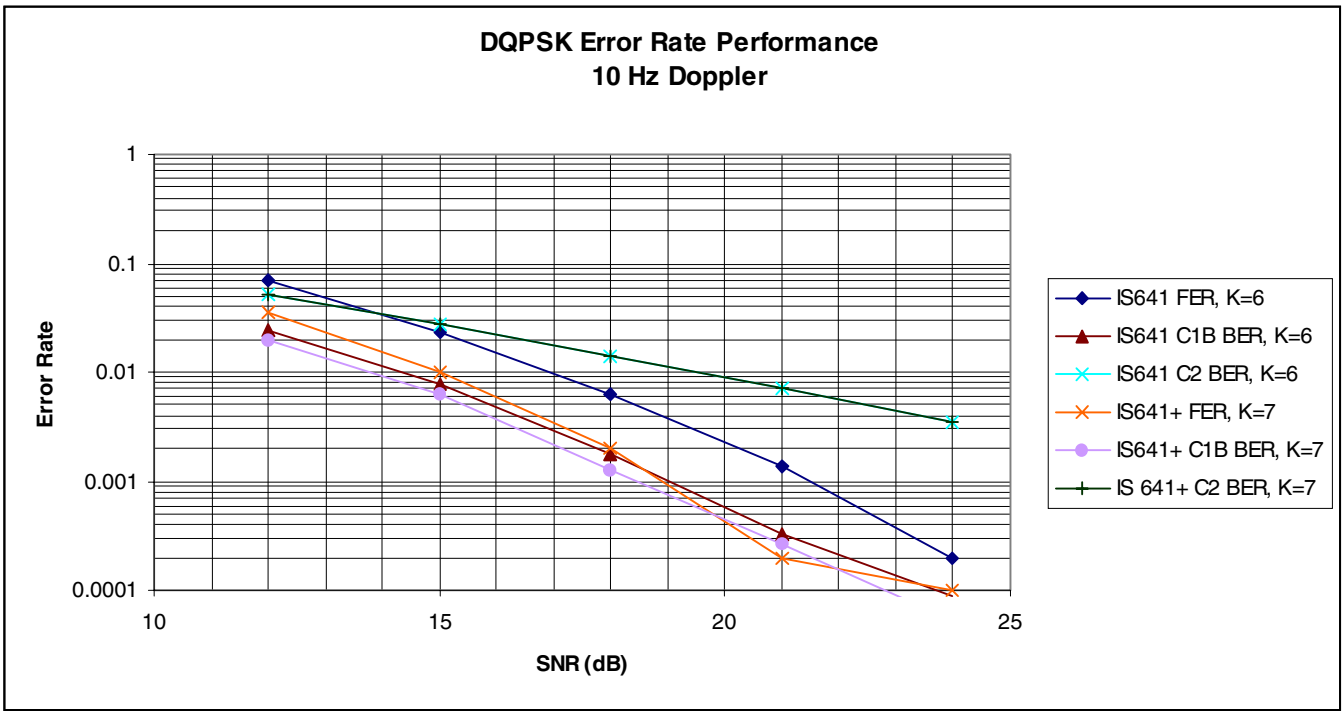

Figure 5. IS641+ Error Rate Performance at 10 Hz Doppler Comparing K=6 with K=7.

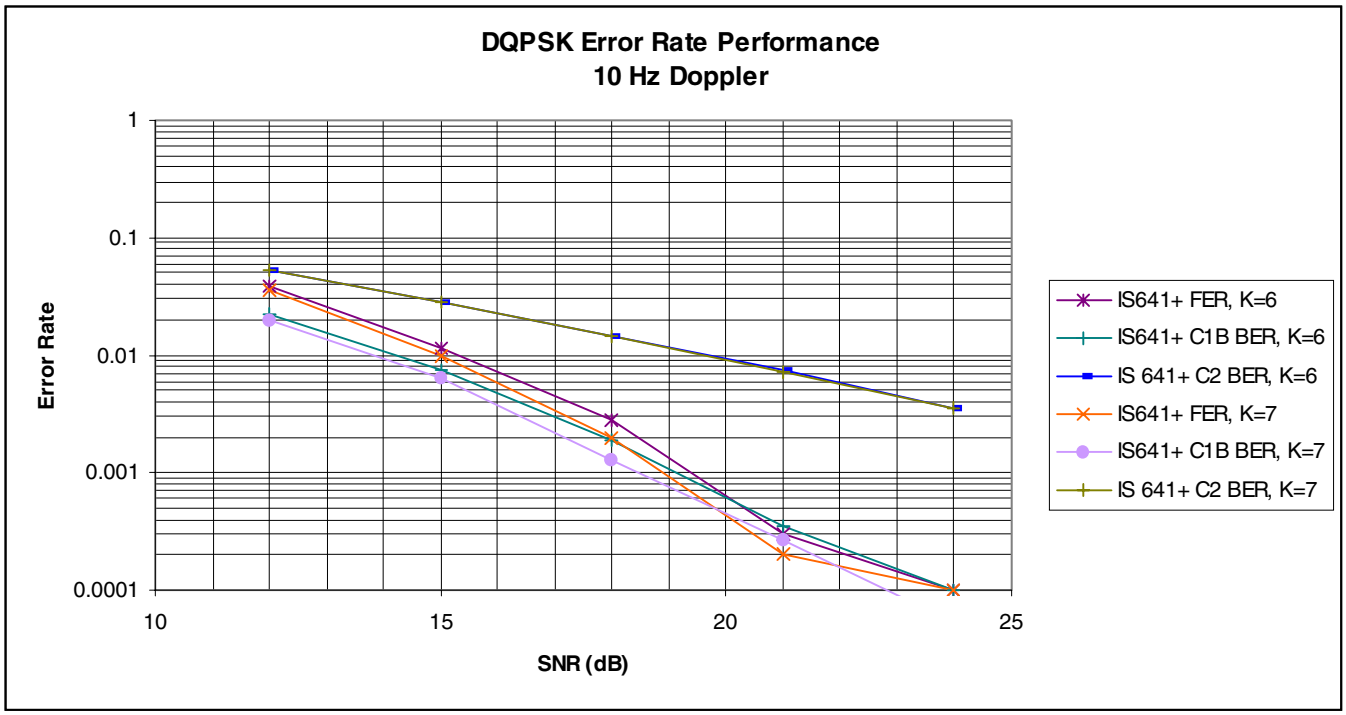

Figure 6. IS641+ Error Rate Performance at 60 Hz Doppler with K=6.

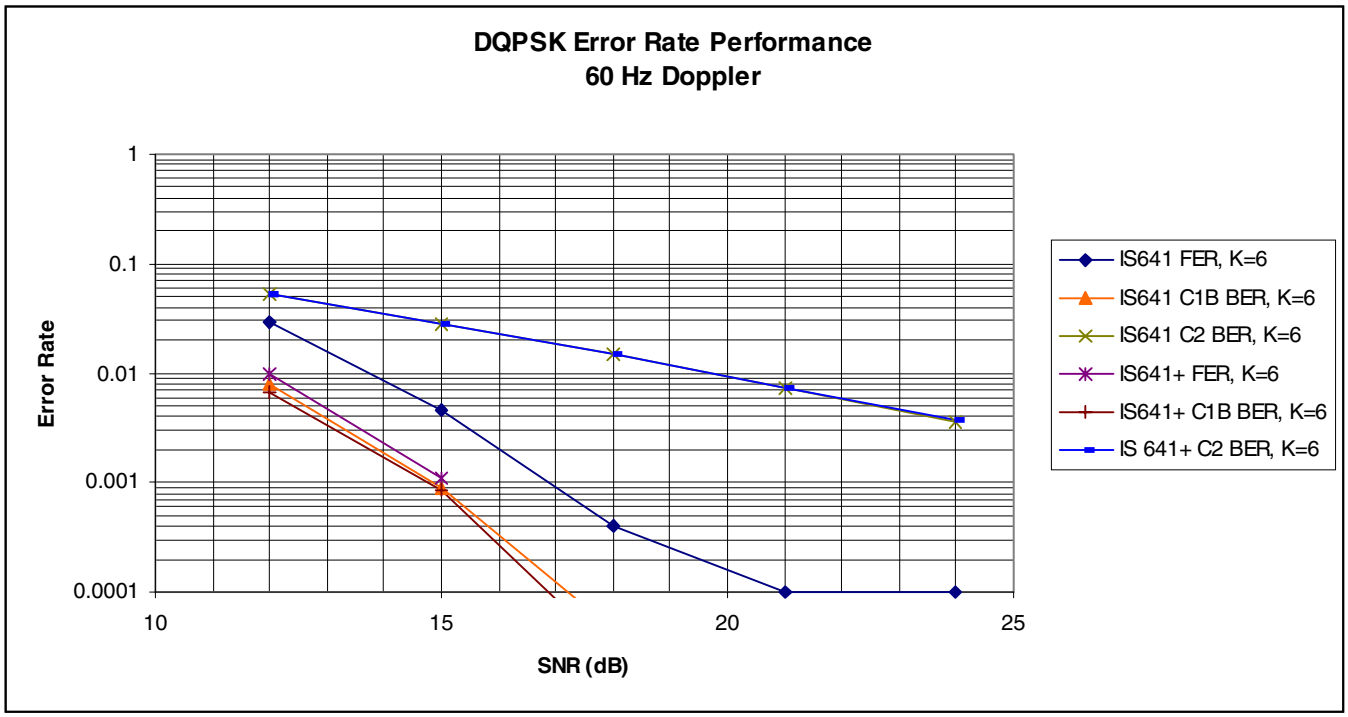

Figure 7. IS641+ Error Rate Performance at 60 Hz Doppler with K=7.

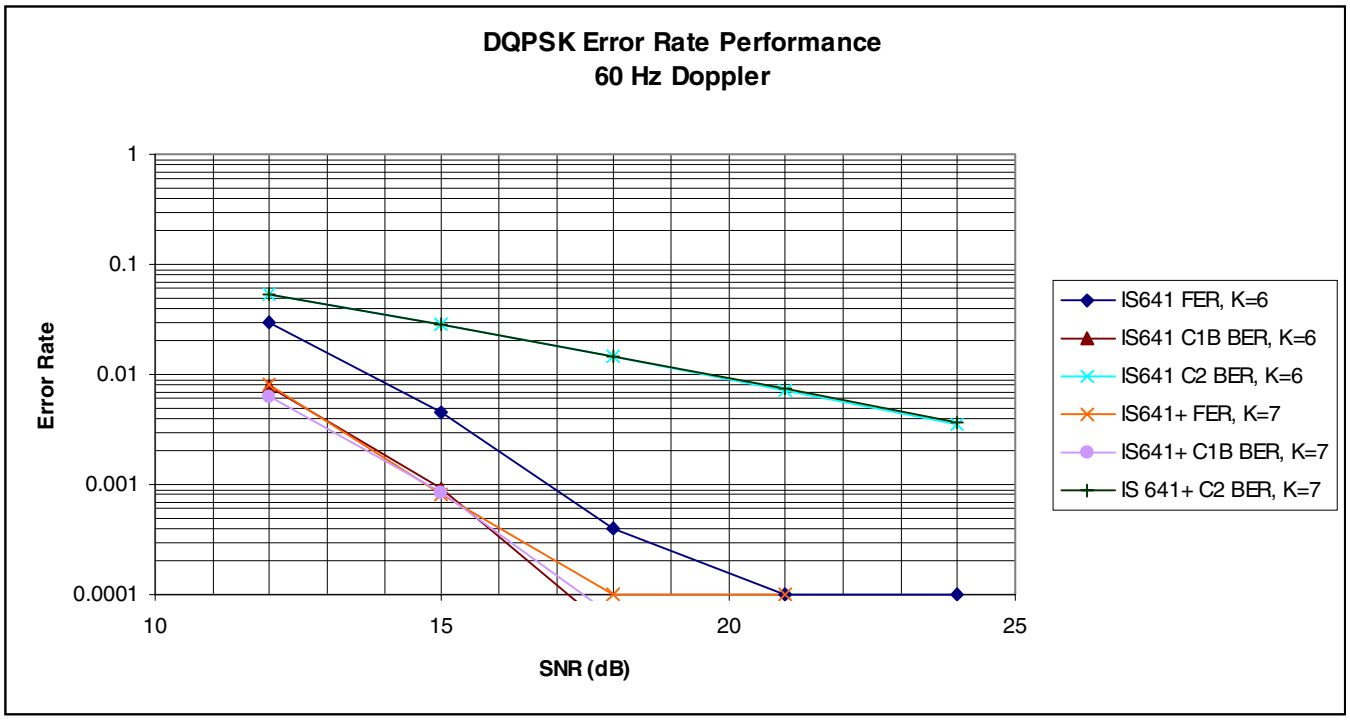

Figure 8. IS641+ Error Rate Performance at 60 Hz Doppler Comparing K=6 with K=7.

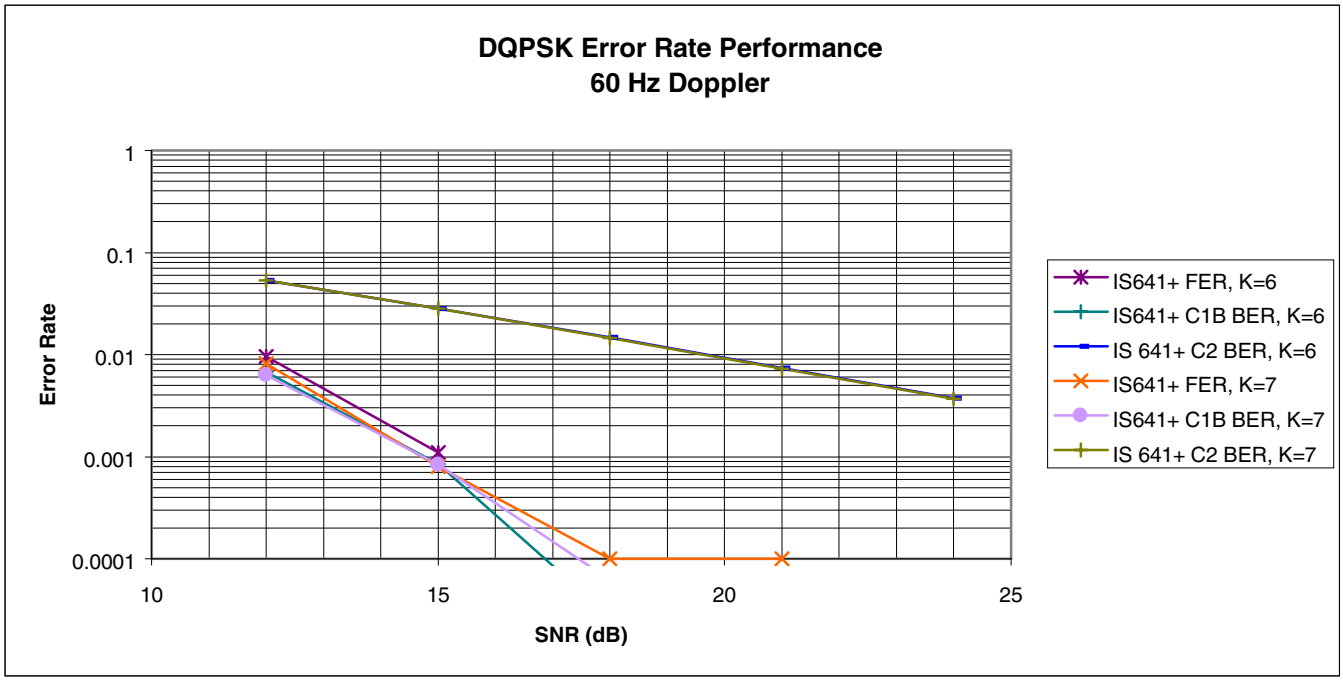

Figure 9. IS641+ Error Rate Performance at 170 Hz Doppler Comparing with K=6.

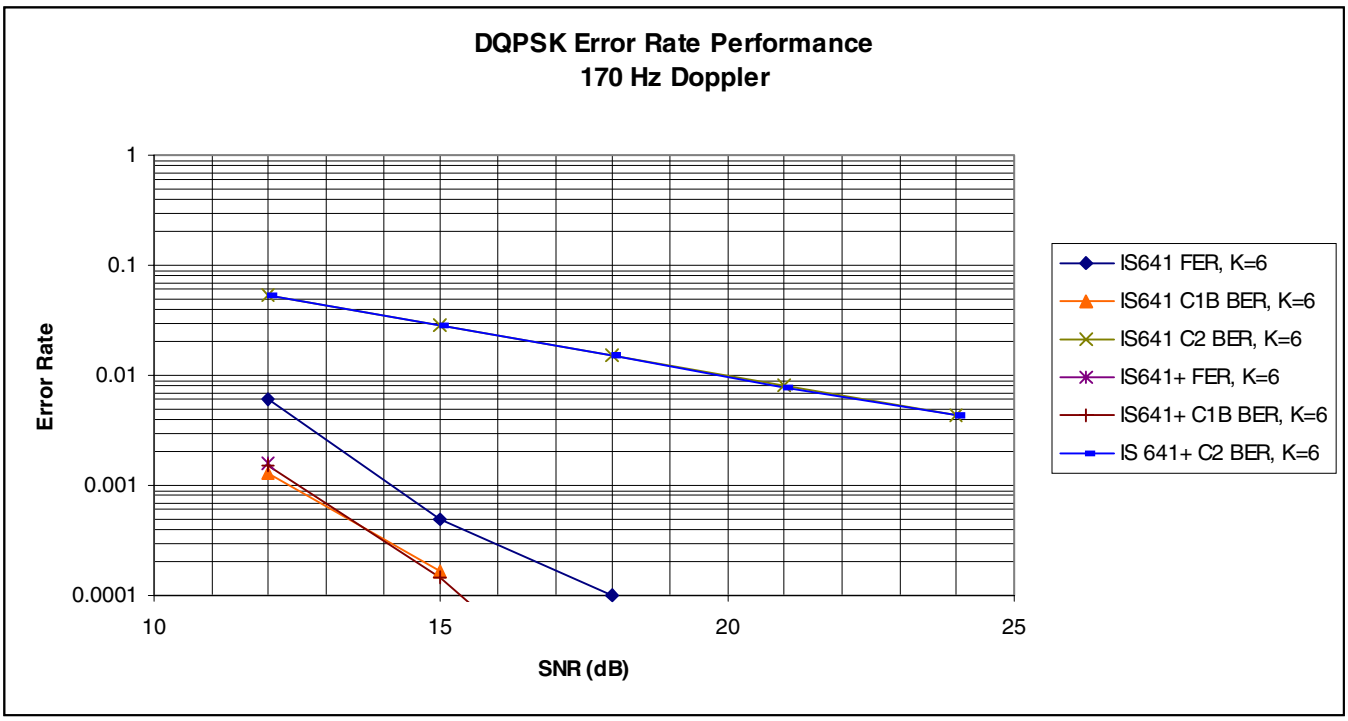

Figure 10. IS641+ Error Rate Performance at 170 Hz Doppler with K=7.

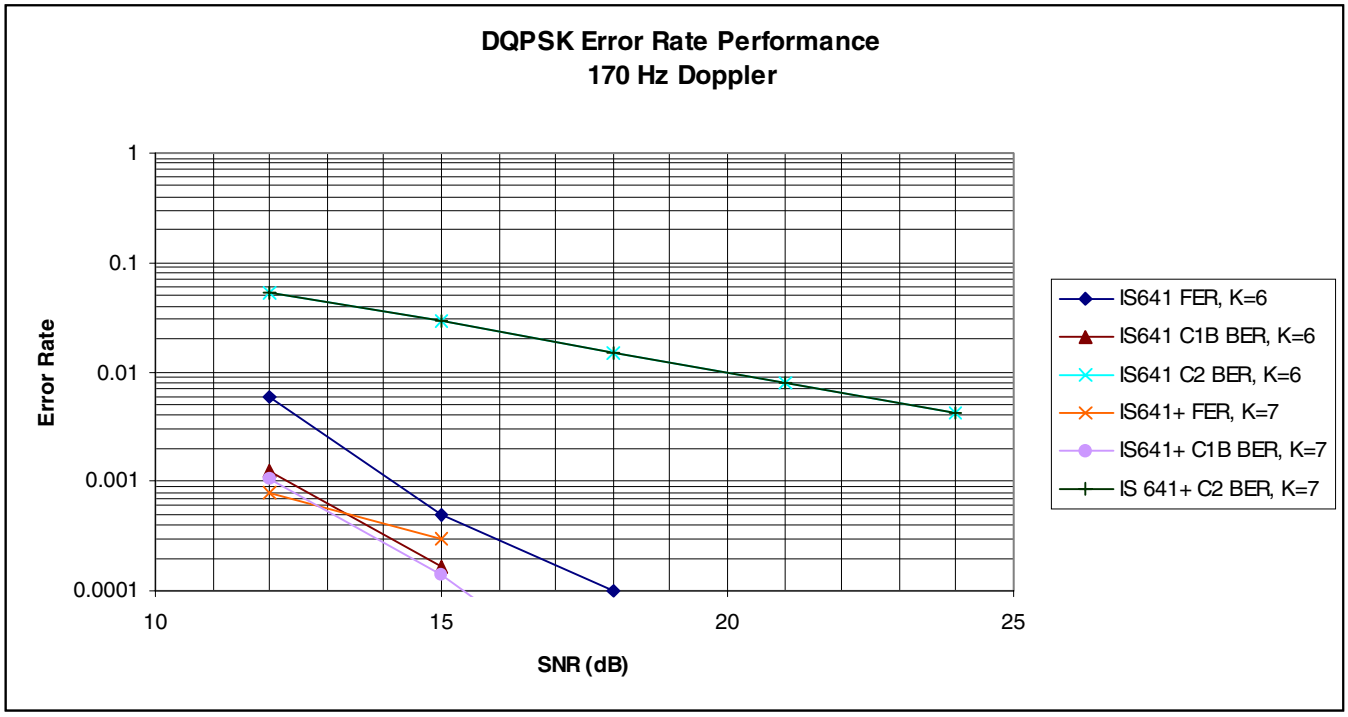

Figure 11. IS641+ Error Rate Performance at 170 Hz Doppler Comparing K=6 with with K=7.